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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,938	02/11/2004	Sunil Talwar	1365.065US1	2395

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER	
FLANAGAN, KRISTA M	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,938	TALWAR ET AL.	
	Examiner	Art Unit	
	Krista M. Flanagan	~~2831~~ 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1, 4, 5, 8, 9, 11, 12, 14-16, 18-20, 22, 23, 25, 26, 28, 29, 31, 32, 34-37, 39, 40, 42, 43, 45, 46, 48 and 49* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) *2,3,6,7,10,13,17,21,24,27,30,33,38,41,44,47 and 50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/04 & 12/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Examiner acknowledges and has considered all documents on the information disclosure statement dated 11 February 2004 however, several documents have been crossed off the list due to relevancy to the application subject matter.

DETAILED ACTION

1. This application is in condition for allowance except for the following formal matters: drawing and claim objections.

Drawings

2. The drawings are objected to because reference characters '17' and '19' in 'figure 7' are not mention in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2, 3, 6, 7, 10, 13, 17, 21, 24, 27, 30, 33, 38, 41, 44, 47 and 50 are objected to because of the following informalities: It is suggested that the named gates (OAI211, OAI22,

AOI22, AOI21, AOI211, and OAI21) be replaced with their respective logic equations in the claims to standardize the claim language. Appropriate correction is required.

Allowable Subject Matter

4. Claims 1, 4, 5, 8, 9, 11, 12, 14-16, 18-20, 22, 23, 25, 26, 28, 29, 31, 32, 34-37, 39, 40, 42, 43, 45, 46, 48 and 49 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

a. Regarding claim 1, prior art fails to disclose a logic circuit comprising two logic levels, the first level logic comprising two logic parts, each logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving the binary inputs and two first level outputs and the second level logic comprising four second level outputs, four second level inputs for receiving second level binary inputs and connected to the four first level outputs, a NAND gate, a first gate generating a logical OR combination of two second level binary inputs and NAND combining the logical OR combination with two other second level binary inputs, a second gate generating logical OR combinations of two pairs of second level binary inputs and NAND combining the logical OR combinations, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

b. Regarding claim 5, prior art fails to disclose a logic circuit comprising two logic levels, the first level logic comprising two logic parts, each logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving the binary inputs and two first level outputs and the second level logic comprising four second level outputs, four second level inputs for receiving second level binary inputs and connected

to the four first level outputs, a NAND gate, a first gate generating logical AND combinations of two pairs of second level binary inputs and NOR combining the logical AND combinations, a second gate generating logical OR combinations of two pairs of second level binary inputs and NAND combining the logical OR combinations, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

c. Regarding claim 9, prior art fails to disclose a logic circuit comprising two logic levels, the first level logic comprising two logic parts, a first logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving two of the binary inputs and two first level outputs, and a second logic part comprising an inverter having one first level logic input for receiving one of the binary inputs and one first level output and the second level logic comprising three second level outputs, and three second level inputs for receiving second level binary inputs and connected to the three first level outputs, a NAND gate, a gate generating a logical AND combination of two second level binary inputs and NOR combining the logical AND combination with one other second level binary input, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

d. Regarding claim 12, prior art fails to disclose a logic circuit comprising: first level logic comprising two logic parts, a first logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving two of the binary inputs and two first level outputs, and a second logic part comprising an inverter having one first level logic input for receiving one of the binary inputs and one first level output and the

second level logic comprising three second level outputs, and three second level inputs for receiving second level binary inputs and connected to the three first level outputs, a NAND gate, a gate generating a logical OR combination of two second level binary inputs and NAND combining the logical OR combination with one other second level binary input, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

e. Regarding claim 15, prior art fails to disclose a logic circuit having seven binary inputs, the logic circuit comprising: first logic for generating a first binary value as a threshold function which is high if at least four binary inputs are high, a second binary value as a threshold function which is high if less than two binary inputs are high, and a third binary value as a threshold function which is high if less than six binary inputs are high; and second logic for forming the OR combination of the first binary value and the second binary value and for NAND combining the third binary value and the result of the OR combination where NAND combining is used to save silicon space and to provide faster processing.

f. Regarding claim 34, prior art fails to disclose a logic circuit having seven binary inputs, the logic circuit comprising: first logic for generating a first binary value as a threshold function which is high if at least four binary inputs are high, a second binary value as a threshold function which is high if less than two binary inputs are high, and a third binary value as a threshold function which is high if less than six binary inputs are high; and an inverting multiplexer to select and output the inverse of the second or third

binary value dependant upon the first binary value where NOR combining is used to save silicon space and to provide faster processing.

Conclusion

6. Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

7. A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Flanagan
20050705

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800